

Micromachined CMOS LNA and VCO By CMOS-Compatible ICP Deep Trench Technology

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Abstract—Selective removal of the silicon underneath the inductors in RF integrated circuits based on inductively coupled plasma (ICP) deep trench technology is demonstrated by a complementary metal–oxide–semiconductor (CMOS) 5-GHz low-noise amplifier (LNA) and a 4-GHz voltage-controlled oscillator (VCO). Design principles of a multistandard LNA with flat and low noise figures (NFs) within a specific frequency range are also presented. A 2-dB increase in peak gain (from 21 to 23 dB) and a 0.5-dB (from 2.28 to 1.78 dB) decrease in minimum NF are achieved in the LNA while a 3-dB suppression of phase noise is obtained in the VCO after the ICP backside dry etching. These results show that the CMOS-process-compatible backside ICP etching technique is very promising for system-on-a-chip applications.

Index Terms—Complementary metal–oxide–semiconductor (CMOS), inductively coupled plasma (ICP), low-noise amplifier (LNA), voltage-controlled oscillator (VCO).

I. INTRODUCTION

RECENTLY, many complementary metal–oxide–semiconductor (CMOS) cascode low-noise amplifiers (LNAs) with excellent performances have been reported [1]–[4]. A review of these works reveals that most of the state-of-the-art LNAs use off-chip bond-wire inductors for input impedance matching [1], [3], [4]. In order to further reduce the form factor and assembly cost toward the goal of a system-on-a-chip (SOC), it is imperative to have the matching network on-chip to embrace the advent and advance of flip-chip technology. However, the quality factor (Q factor) of on-chip inductors is low due to the losses in the conductive silicon substrate as well as the series resistance of the metallization. Various methods have been proposed to enhance the Q factor, such as high-resistivity silicon [5], front-side and backside micromachining [6]–[10], porous silicon [11], [12], proton implantation [13], and patterned ground shields (PGSs) [14]. Only

very few of them have verified their high- Q inductors in RF active circuits. This is because most of the proposed methods are very difficult, if not impossible, to integrate into standard CMOS technology due to their inherent nonstandard CMOS processing steps. In addition, the front-side etching has inherent limitations as to how far circuits can be placed from the inductors [7]. The PGS method, while it is compatible with CMOS technology, has the drawbacks of limited improvement of Q and reduction of self-resonant frequency (f_{SR}). Fortunately, these problems can be largely improved by our proposed CMOS-compatible backside inductively coupled plasma (ICP) dry etching technology.

In this study, the CMOS-compatible backside ICP deep trench technology, which selectively removes the conductive silicon substrate underneath the inductors in CMOS RF integrated circuits, is demonstrated. In Section II, the detailed process steps of the backside ICP deep trench technology are introduced. In Section III, design principles of a multistandard LNA with flat and low noise figures (NFs) within a specific frequency range are presented for the first time. In Section IV, a 5.15–5.825-GHz multistandard CMOS LNA, and a 4-GHz low-phase noise CMOS voltage-controlled oscillator (VCO) are designed. The LNA and the VCO were implemented in standard 0.25- and 0.18- μm CMOS technologies, respectively, provided by the commercial foundry UMC. In Section V, the LNA and the VCO before and after ICP dry etching are measured and analyzed. Section VI presents the conclusions.

II. DEEP TRENCH TECHNOLOGY

The processing steps of our backside ICP deep trench technology shown in Fig. 1 are described as follows. First, the front-side (the side with the LNA/VCO) of the finished die was attached to a glass substrate with adhesive wax followed by mechanical lapping, which thinned the silicon substrate down to about 100 μm . Second, the wax was softened by heating, so that the glass substrate in the front-side of the die could be removed. Then, the front-side of the die was cleaned with acetone. Third, the front-side of the 100- μm -thick die was stuck to a glass substrate with adhesive S1813 followed by dropping photoresist SU8 on the backside of the sample. After standard photolithography processes on the backside of the die, the ICP dry etching was used to remove the silicon underneath the inductors of the LNA/VCO. The main gases used during the ICP etching process were an alternate cycle of SF_6 (for etching) and C_4F_8 (for passivation), which took approximately 17 s. The ICP etching rate

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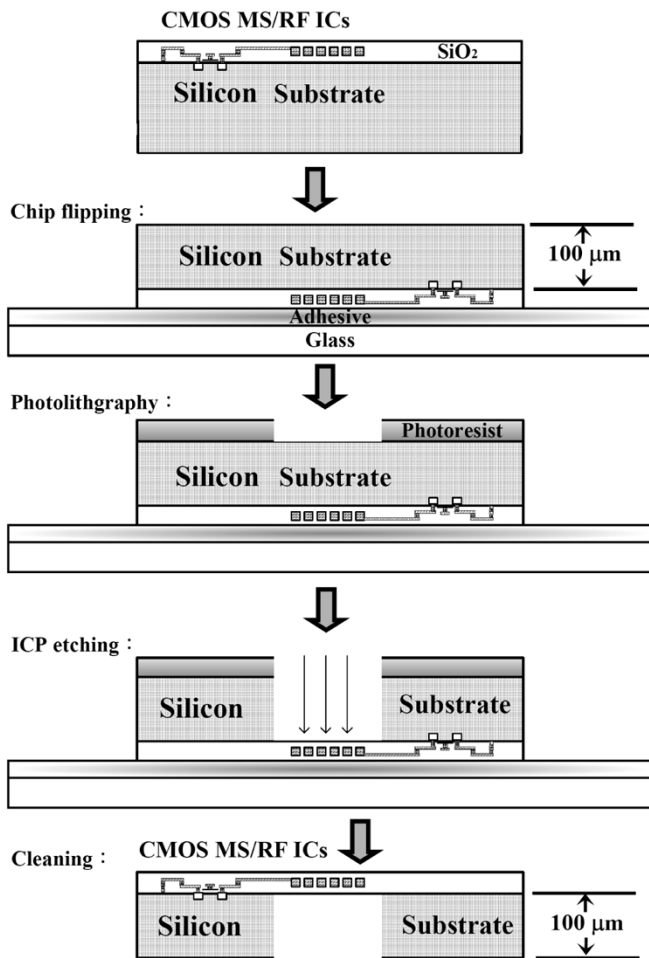


Fig. 1. Process steps of the backside ICP deep trench etching technology.

was about $2 \mu\text{m}/\text{min}$, so the total etching time was approximately 50 min. Finally, the adhesive and photoresist which covered the front-side and backside of the die, respectively, were removed for test purposes.

A 5.15–5.825-GHz multistandard CMOS LNA and a 4-GHz CMOS VCO with schematics shown in Figs. 2(a) and 3(a), respectively, have gone through this backside ICP dry etching. The front-side die photographs of the LNA and the VCO before ICP dry etching are shown in Figs. 2(b) and 3(b), respectively. The backside die photographs of the LNA and the VCO after ICP dry etching are shown in Figs. 2(c) and 3(c), respectively, where the exposed front-side on-chip inductors are visible to the naked eye and the sidewalls of the “drilled” or micromachined holes are virtually vertical. Compared with the traditional backside wet bulk micromachining, the dry ICP etching has the advantages of forming vertical sidewalls and being fully CMOS process compatible since it is a standard processing technique in modern CMOS technology.

III. PRINCIPLES OF MULTISTANDARD CMOS LNA DESIGN

A multistandard low-noise LNA should attain a good input matching (i.e., $20 \log |S_{11}| \leq -10 \text{ dB}$) and a flat and low NF performance over the frequency band of interest. To achieve wide-band input matching, the frequency response of the input

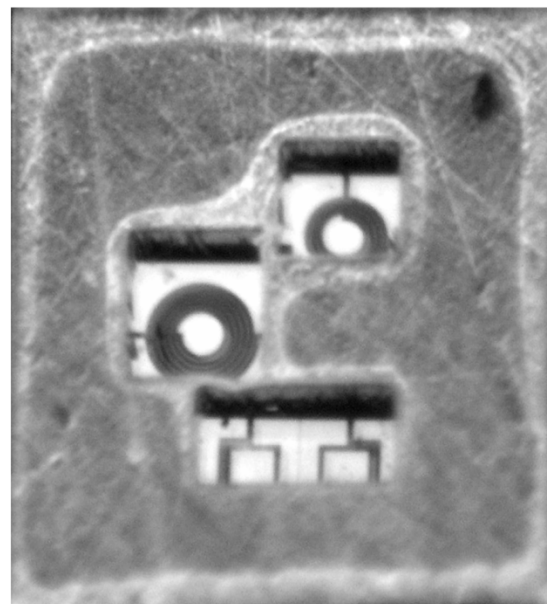
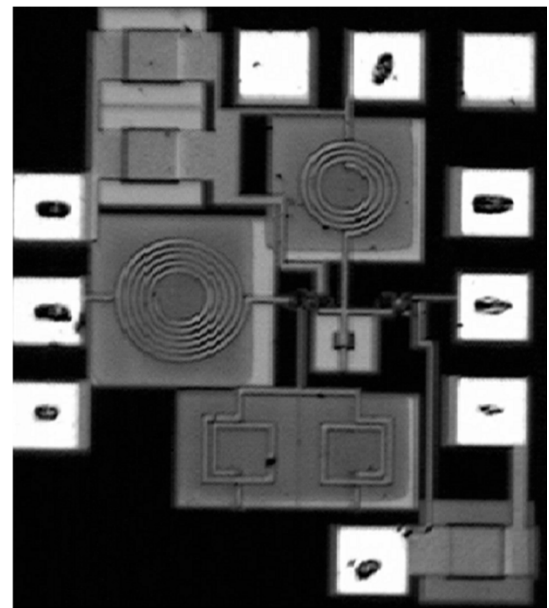
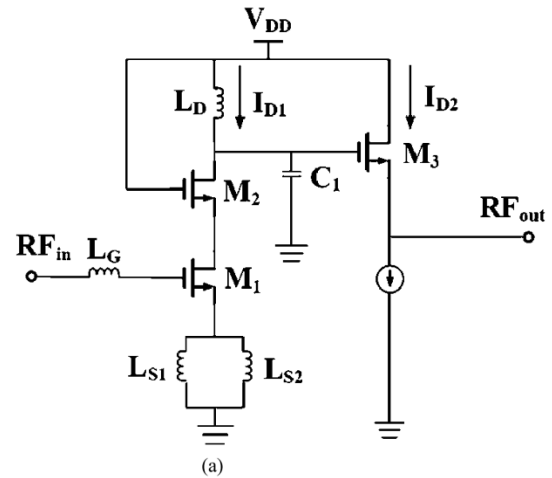


Fig. 2. (a) Schematic, (b) front-side die photograph, and (c) backside die photograph of the 5.15–5.825-GHz multistandard CMOS LNA.

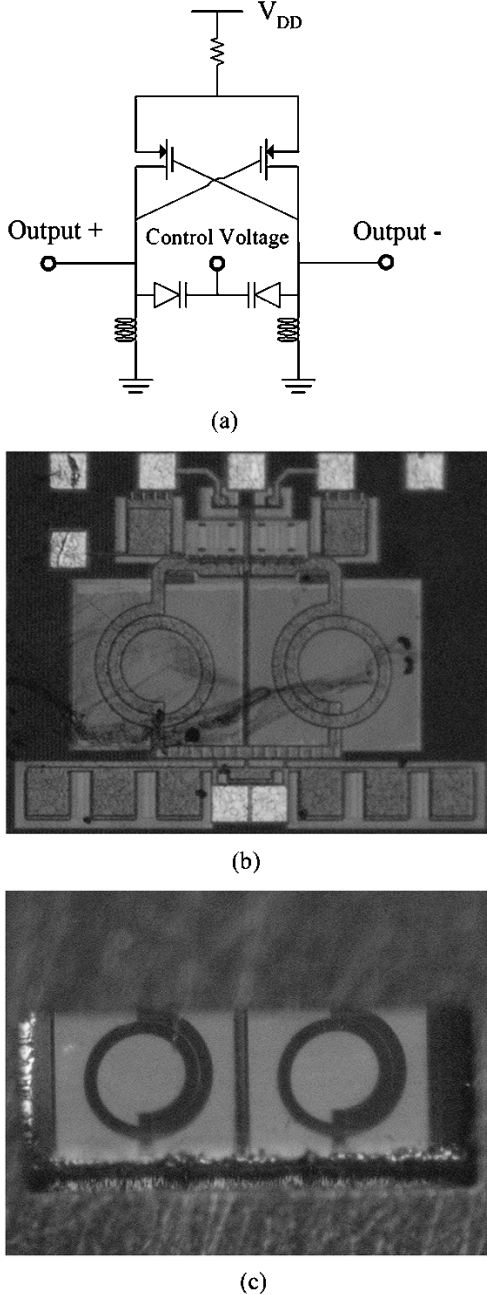


Fig. 3. (a) Schematic, (b) front-side die photograph, and (c) backside die photograph of the 4-GHz CMOS LC VCO.

return loss S_{11} has to be derived first. According to Fig. 2(a), the input impedance Z_{in} of a cascode LNA is given by

$$Z_{in} \approx s(L_G + L_S) + \frac{g_{m1}L_S}{C_{gs1}} + \frac{1}{s(kC_{gs1})} \quad (1)$$

in which g_{m1} is the transconductance, C_{gs1} is the gate-source capacitance of transistor M_1 , and k is a correction factor that takes into accounts the Miller capacitance contributed by C_{gd1} , i.e., the gate-drain capacitance of M_1 . The value of k is about 1.61 for the 0.25- μm CMOS technology used. The source-degenerative inductance L_S can be determined by the following equation:

$$R_S = \frac{g_{m1}L_S}{C_{gs1}} = 50 \Omega. \quad (2)$$

According to (1), the input return loss S_{11} can be expressed as

$$\begin{aligned} S_{11} &= \frac{Z_{in} - R_S}{Z_{in} + R_S} \\ &= \frac{s(L_G + L_S) + \frac{1}{s(kC_{gs1})}}{s(L_G + L_S) + 2 \cdot \frac{g_{m1}L_S}{C_{gs1}} + \frac{1}{s(kC_{gs1})}} \\ &= \frac{s^2 + \frac{1}{kC_{gs1}(L_G + L_S)}}{s^2 + 2 \cdot \frac{g_{m1}L_S}{C_{gs1}(L_G + L_S)} \cdot s + \frac{1}{kC_{gs1}(L_G + L_S)}} \\ &= \frac{s^2 + \omega_o^2}{s^2 + Bs + \omega_o^2} \\ &= \frac{s^2 + \omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \end{aligned} \quad (3)$$

in which

$$\omega_o^2 \equiv \frac{1}{kC_{gs1}(L_G + L_S)} \quad (4)$$

$$\begin{aligned} B &\equiv 2 \cdot \frac{g_{m1}L_S}{C_{gs1}(L_G + L_S)} \\ &\approx \frac{100}{(L_G + L_S)} \end{aligned} \quad (5)$$

$$\begin{aligned} Q &\equiv \frac{\omega_o}{2R_S}(L_G + L_S) \\ &= \frac{1}{2\omega_o k C_{gs1} R_S} \\ &\equiv \frac{Q_L}{2k} \\ &\approx \frac{Q_L}{3.22}. \end{aligned} \quad (6)$$

Note that the Q in (6) is proportional to the Q_L defined by Shafer and Lee [15]. By plugging $s = j\omega$ into (3), $|S_{11}|$ can be expressed as

$$|S_{11}| = \left| \frac{-\omega^2 + \omega_o^2}{-\omega^2 + j\omega B + \omega_o^2} \right|. \quad (7)$$

Now, it is clear that $|S_{11}|$ is a standard notch function with -3 -dB matching bandwidth equal to B (or $100/(L_G + L_S)$) [16]. In general, $|S_{11}|$ should be smaller than -10 dB over the band of interest, i.e.,

$$20 \log |S_{11}| \leq -10 \text{ dB}. \quad (8)$$

By substituting the expression of $|S_{11}|$ in (7) into (8) and after some calculations, the solutions of ω that satisfy (8) can be obtained as follows:

$$\frac{-B + \sqrt{B^2 + 36\omega_o^2}}{6} \leq \omega \leq \frac{B + \sqrt{B^2 + 36\omega_o^2}}{6}. \quad (9)$$

Therefore, the corresponding matching bandwidth Δf is equal to

$$\Delta f = \frac{\Delta\omega}{2\pi} = \frac{B}{6\pi} \approx \frac{50}{3\pi \cdot (L_G + L_S)}. \quad (10)$$

The above theory sets an upper limit for the total inductance of the inductors connected to the input transistor or Q_L with a desired input matching bandwidth of Δf . That is, if the total inductance or Q_L is too large, the requirement for the input-matching bandwidth will not be satisfied. Fig. 4(a) shows the calculated $|S_{11}|$ versus frequency characteristics of a 5-GHz-band CMOS LNA (with various inductance inductors ($L_G + L_S$))

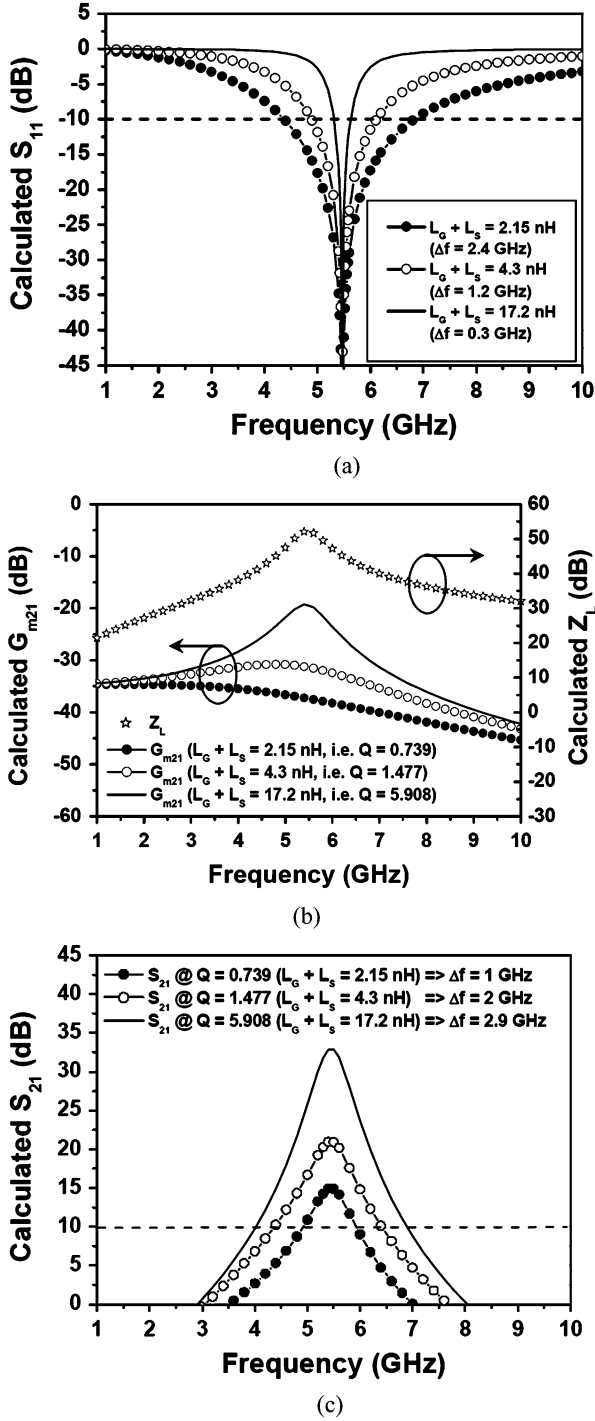


Fig. 4. Simulated: (a) input-matching (S_{11}), (b) transconductance gain $G_{m21}(s)$, load impedance $Z_L(s)$, and (c) gain (S_{21}) of a 5-GHz-band CMOS cascode LNA with various inductance inductors ($L_G + L_S$) connected to the input transistor.

connected to the input transistor) by using (7). The center frequency $f_o (= \omega_o/2\pi)$ is set as 5.467 GHz because it can be defined as the geometric mean of the targeted band-edge frequencies, which are 4.9 and 6.1 GHz, respectively, in this example. As can be seen, matching bandwidth Δf decreases with the increase of inductance of $L_G + L_S$ (or Q_L), which is consistent with (10). From a power-constrained NF condition [15], it is pointed out that Q_L should less than 5.5. Consequently, in order to simultaneously satisfy the requirements of sufficient

wide input-matching bandwidth, low power, and low noise, the upper limit of the total inductance of the inductors connected to the input transistor or Q_L should be set by (10) or $Q_L = 5.5$ depending on which is smaller.

In the following, we discuss the lower limit for the total inductance of the inductors connected to the input transistor or Q_L . If we only consider the transfer function of S_{11} , it seems that we can pick a very small total inductance to achieve a very broad bandwidth. One of the corresponding drawbacks is that the Q_L value of the input circuit will be even lower than the lower limit (3.5) of Q_L set by the power-constrained NF condition [15]. Therefore, we conclude that lower limit for the total inductance of the inductors connected to the input transistor or Q_L should be set by $Q_L = 3.5$ while the upper limit should be set by (10) or $Q_L = 5.5$ depending on which is smaller. Furthermore, if gain S_{21} is taken into account, we will see that a new lower limit of Q_L or total inductance of the inductors connected to the input transistor can be determined given that the input matching bandwidth is first satisfied. From the expressions of S -parameters in terms of Z - or Y -parameters [17], it is found that the denominators, or the poles, of all S -parameters are the same. With the information of poles and zeros plus dc or mid-band gain, the frequency response of voltage gain, or S_{21} , of a circuit can be obtained easily [18]. For the cascode LNA circuit shown in Fig. 2(a), the transfer function of S_{21} can be derived as follows:

$$\begin{aligned}
 S_{21} &= 2 \cdot \frac{v_{\text{out}}}{v_{\text{sig}}} \\
 &= 2 \cdot \frac{v_{\text{out}}}{v_{g3}} \cdot \frac{v_{g3}}{v_{\text{sig}}} \\
 &\approx 2 \cdot \frac{v_{g3}}{v_{\text{sig}}} \\
 &= \frac{-2g_{m1}\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \cdot \frac{1}{1 + \frac{s}{\omega_{M2}}} \cdot \frac{r\omega_{o1}^2 + sL\omega_{o1}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \\
 &\approx \frac{-2g_{m1}\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \cdot \frac{r\omega_{o1}^2 + sL\omega_{o1}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \\
 &\equiv \frac{-2g_{m1}\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \cdot Z_L(s) \\
 &\equiv G_{m21}(s) \cdot Z_L(s)
 \end{aligned} \tag{11}$$

in which $\omega_{M2} \equiv g_{m2}/C_{gs2}$, $\omega_{o1}^2 \equiv 1/L(C_1 + C_{gs3})$, and $Q_1 \equiv (\omega_{o1}L)/r$. In addition, r and L represent the equivalent series resistance and inductance of inductor L_D , respectively. $G_{m21}(s)$ represents the transconductance gain if the input voltage adopts the input-terminal voltage (i.e., $v_{\text{sig}}/2$). $Z_L(s)$ represents the equivalent load impedance seen at the drain terminal of the transistor M2.

Fig. 4(b) and (c) shows the calculated $|G_{m21}(s)|$ and $|Z_L(s)|$, and $|S_{21}|$ (i.e., $|G_{m21}(s) \cdot Z_L(s)|$) versus frequency characteristics of a 5-GHz-band CMOS LNA (with various inductance inductors ($L_G + L_S$) connected to the input transistor) by using (11). As can be seen, an input matching with low $Q(Q_L)$ value will degrade gain. Therefore, the $Q(Q_L)$ value should not be lower than 1.414 (4.552), which corresponds to a maximum flat response in the first part (i.e., $|G_{m21}(s)|$) of the transfer function of $|S_{21}|$.

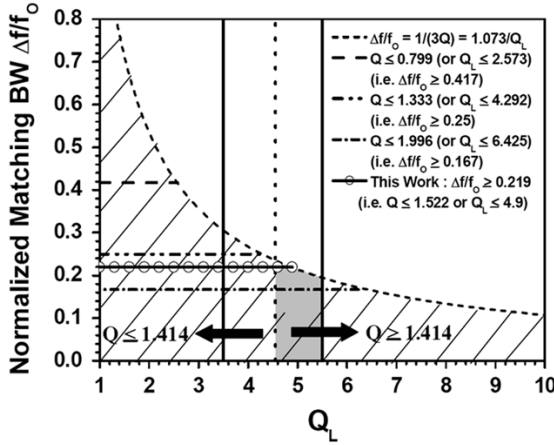


Fig. 5. Calculated normalized matching bandwidth $\Delta f/f_o$ versus Q_L characteristics of a CMOS cascode LNA.

Based on (6) and (10), we can obtain a design equation with normalized input-matching bandwidth $\Delta f/f_o$ of CMOS cascode LNAs for the upper limit of the total inductance of the inductors connected to the input transistor or Q_L as follows:

$$\frac{\Delta f}{f_o} = \frac{1}{3Q} \approx \frac{1.073}{Q_L}. \quad (12)$$

Fig. 5 shows the calculated normalized input matching bandwidth $\Delta f/f_o$ versus Q_L characteristics based on (12). To meet the specification of the input-matching bandwidth Δf , the design point should fall into the area marked by the oblique lines. The constraints of Q_L (3.5 and 5.5) according to the power-constrained noise theory of Shaeffer and Lee [15] are also shown in Fig. 5. In addition, as mentioned before, to achieve a maximum flat response in the first part (i.e., $|G_{m21}(s)|$) of the transfer function of $|S_{21}|$, the Q value should not be lower than 1.414. That is, Q_L should not be lower than 4.552 for the 0.25- μm CMOS technology used. Therefore, the lower limit for the total inductance of the inductors connected to the input transistor or Q_L should be set by $Q_L = 4.552$ while the upper limit should be set by (12) or $Q_L = 5.5$, depending on which is smaller, as is illustrated in Fig. 5.

The gray region in Fig. 5 bounded by $Q_L = 4.552$, $Q_L = 5.5$, and (12) represents a very interesting area with low noise, low power consumption, and high gain. The corresponding $\Delta f/f_o$ range is from 0.195 to 0.236 according to (12). This means that, for a given technology, only a specific range of $\Delta f/f_o$ leads to a low and flat NF performance over the band of interest with low power consumption and high gain. If the specified $\Delta f/f_o$ is outside this range, i.e., its corresponding Q_L is not between 4.55–5.5, a tradeoff between $\Delta f/f_o$, NF, power consumption, and gain will be made.

Consider the four cases indicated in Fig. 5. First, if the required input-matching bandwidth $\Delta f/f_o$ is 0.417, then it is impossible to achieve a very low and flat NF performance over the band of interest with low power consumption because all of the Q_L values ($Q_L \leq 2.573$) that satisfy the input-matching bandwidth requirement do not fall into the range of $3.5 \leq Q_{L,\text{opt}} \leq 5.5$, as shown in Fig. 5. For this case, the design point

should be chosen at $Q_L = 2.573$ because the corresponding Q_L value is closer to the $Q_{L,\text{opt}}$ range. Second, if the required input-matching bandwidth $\Delta f/f_o$ is 0.25, then the upper limit of Q_L is 4.292 according to (12), because it is smaller than 5.5 while the lower limit of Q_L is 3.5. For this case, choosing a Q_L within $3.5 \leq Q_{L,\text{opt}} \leq 4.292$ can achieve a low and flat NF performance over the band of interest with low power consumption but without optimum gain. Third, if the required input-matching bandwidth $\Delta f/f_o$ is 0.167, then the upper limit of Q_L is 5.5 because it is smaller than 6.425 calculated by (12), while the lower limit of Q_L is 4.552 instead of 3.5 to achieve a better gain. For this case, choosing a Q_L within $4.552 \leq Q_{L,\text{opt}} \leq 5.5$ can achieve a low and flat NF performance over the band of interest with low power consumption and optimum gain. Finally, for the 4.9–6.1-GHz multistandard CMOS LNA studied in this work, the required input-matching bandwidth Δf is at least 1.2 GHz, i.e., $\Delta f/f_o \geq 0.219$ if the center frequency f_o is set as 5.467 GHz. The upper limit of Q_L is 4.9 according to (12) because it is smaller than 5.5 while the lower limit of Q_L is 4.552 instead of 3.5 to achieve a better gain. For this case, choosing a Q_L within $4.552 \leq Q_{L,\text{opt}} \leq 4.9$ can achieve a low and flat NF performance over the band of interest with low power consumption and optimum gain. A more detailed discussion regarding the design of the 5.15–5.825-GHz multistandard CMOS LNA studied in this work will be given in Section IV.

IV. CIRCUIT DESIGN

A. 5.15–5.825-GHz Multistandard CMOS LNA

Fig. 2(a) shows the schematic diagram of our CMOS LNA targeted to cover the multistandards of 802.11a or Wimax with frequency ranges of 5.15–5.35 and 5.725–5.825 GHz. The input-matching bandwidth (i.e., the frequency range that satisfies $20 \log |S_{11}| \leq -10$ dB) in design is chosen to be 1.2 GHz (i.e., from 4.9 to 6.1 GHz) to accommodate possible frequency shift due to process variation. The center frequency $f_o (= \omega_o/2\pi)$ is set as 5.467 GHz because it is defined as the geometric mean of the band-edge frequencies, i.e., 4.9 and 6.1 GHz. The LNA was implemented in a standard 0.25- μm CMOS process. Basically, this multistandard CMOS LNA is a cascode amplifier (M1 and M2) with two parallel-connected source-degenerative inductors (L_{S1} and L_{S2}) and one gate inductor L_G for simultaneous input impedance and noise-matching. L_D and C_1 function as the tuned load. A source follower composed of M3 and a current source was used as a buffer for test purposes [19]. To achieve flat and low NF versus frequency characteristics over the frequency band of interest, the theory introduced in Section III was used to determine the inductances of on-chip inductors L_G , L_{S1} , and L_{S2} , and the device size of transistor M1 of this multistandard LNA. The circuit parameters are: $L_G = 4.0$ nH, $L_{S1} = L_{S2} = 0.6$ nH, $L_D = 1.5$ nH, $C_1 = 0.3$ pF, transistor size M1: $(W/L)_1 = M2: (W/L)_2 = 110/0.24 \mu\text{m}/\mu\text{m}$, and M3: $(W/L)_3 = 90/0.24 \mu\text{m}/\mu\text{m}$.

The desired matching bandwidth for the LNA shown in Fig. 2(a) is $\Delta f = 1.2$ GHz, i.e., from 4.9 to 6.1 GHz. Based on (10), the corresponding inductance connected to the input

transistor (i.e., $L_G + L_S$, in which $L_S = L_{S1}/2$) should satisfy the following equation:

$$L_G + L_S \leq 4.421 \text{ nH}. \quad (13)$$

In addition, to achieve a maximum flat response in the first part (i.e., $|G_{m21}(s)|$) of the transfer function of $|S_{21}|$, the Q value should not be lower than 1.414. From (6), there exists a lower limit for the total inductance of the inductors connected to the input transistor as follows:

$$L_G + L_S \geq 4.116 \text{ nH}. \quad (14)$$

Combining (13) and (14), we can conclude that, for a multistandard LNA with matching bandwidth from 4.9 to 6.1 GHz, the total inductance of the inductors connected to the input transistor should satisfy the following equation:

$$4.116 \text{ nH} \leq L_G + L_S \leq 4.421 \text{ nH}. \quad (15)$$

In the design of our LNA, the total inductance of the inductors connected to the input transistor is equal to 4.3 nH, which falls into the range described above. This explains why the requirement of wide-bandwidth input matching and gain can be simultaneously met (see the results shown in Section V). In addition, by plugging the range of $L_G + L_S$ in (15) into (6), we can obtain the corresponding Q_L range as follows:

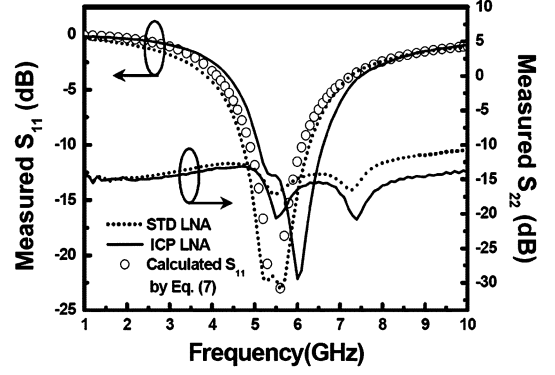
$$4.552 \leq Q_L \leq 4.9 \quad (16)$$

(i.e., $1.2 \text{ GHz} \leq \Delta f(@f_0 = 5.467 \text{ GHz}) \leq 1.289 \text{ GHz}$), which is also shown in Fig. 5. Clearly, this Q_L range falls into the final $Q_{L,\text{opt}}$ range, i.e., from 4.552 to 5.5. This explains why our implemented 5.15–5.825-GHz multistandard LNA can not only meet the requirements of wide-bandwidth (from 4.9 to 6.1 GHz) input matching and gain, but also achieve very flat and low NF performances over the band of interest (see the results shown in Section V).

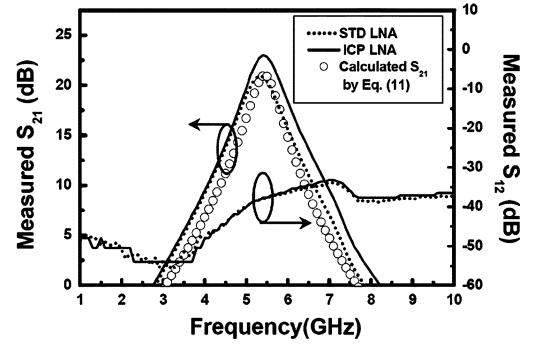
On the other hand, the results of power-constrained noise theory also mean that, if $Q_{L,\text{opt}}$ of the input transistor of a multistandard LNA is around 4.5 (i.e., average of 3.5 and 5.5) at the center frequency (i.e., 5.467 GHz), then the achievable NF over the band of interest will be relatively insensitive to frequency variation [i.e., generally changing by 0.1 dB or less; see Fig. 6(c)]. The optimized size of the input transistor can be determined as follows [15]:

$$W_{\text{OPT}} = \frac{3}{2\omega_o LC_{\text{ox}} R_S Q_{L,\text{opt}}} \approx \frac{1}{3\omega LC_{\text{ox}} R_S} \approx 114.3 \mu\text{m}. \quad (17)$$

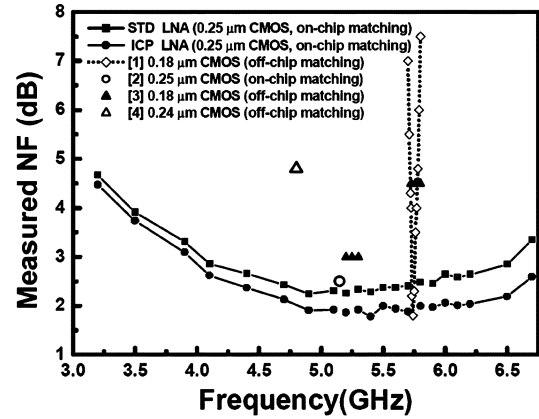
In our design, the device size is $110 \mu\text{m}$, i.e., $Q_L = 4.676$, which is very close to 4.5. This explains again why our implemented 5.15–5.825-GHz multistandard LNA exhibited a very flat and low NF performance over the band of interest (see the results shown in Section V).



(a)



(b)



(c)

Fig. 6. Measured: (a) input-matching (S_{11}) and output-matching (S_{22}), (b) gain (S_{21}) and reverse isolation (S_{12}), and (c) NF of our 5.15–5.825-GHz multistandard CMOS cascode LNA before and after backside ICP dry etching. The measured NF of the previously reported state-of-the-art 5-GHz-band CMOS cascode LNAs are also shown for comparison.

B. 4-GHz CMOS VCO

CMOS voltage-controlled oscillators (VCOs) with integrated inductors are well suited for wireless applications [20], [21]. To prevent the unwanted frequency-pulling effect, a VCO operating at twice the carrier frequency with a following divide-by-two stage can be utilized as the local oscillator in a direct-conversion transceiver. For wireless applications such as dynamic channel selection (DCS), personal communication services (PCSs), and wide-band code-division multiple access (WCDMA), a phase noise of -113 dBc/Hz at 600-kHz offset from the carrier frequency is the minimum requirement for

a 3.8–4.2-GHz VCO. When the operating frequency exceeds 3 GHz, losses caused by the induced eddy current in the silicon substrate begins to degrade the Q factor of inductors. For LC VCOs, the Q of the resonance tank, which is strongly related to the phase noise, will also be pulled down by such a painful loss. Therefore, considerable power consumption is usually necessary to maintain an acceptable phase-noise performance in VCOs.

Fig. 3(a) shows the schematic diagram of our designed 3.9–4.2-GHz monolithic low-phase noise CMOS VCO with 7.5-mW dc power consumption by using the standard 0.18- μm CMOS technology. The circuit parameters are: PMOS transistor size: $W/L = 300 \mu\text{m}/0.34 \mu\text{m}$; resistor size: $W/L = 4 \times 10 \mu\text{m}/40 \mu\text{m}$; varactor size: $W/L = 120 \mu\text{m}/1 \mu\text{m}$; and inductor value = 0.56 nH. The negative conductance required to sustain a stable oscillation is generated by the cross-coupled PMOS pair. Although a NMOS or CMOS topology seems to be more power-saving, VCO cores consisting of NMOS usually suffer from excess $1/f$ noise. To prevent the up-conversion of low frequency noise, the tail current is defined by a polysilicon resistor instead of a field-effect transistor (FET) current source which may contribute considerable $1/f$ noise.

V. RESULTS AND DISCUSSIONS

A. Micromachined 5.15–5.825-GHz CMOS LNA

To verify the effects of backside ICP dry etching on a 5.15–5.825-GHz multistandard CMOS LNA, the CMOS LNA was tested before and after ICP etching. The bias conditions are $V_{DD} = 2.5 \text{ V}$, $I_{D1} = 12 \text{ mA}$, and $I_{D2} = 3 \text{ mA}$. Measured input and output return losses (S_{11} and S_{22}) of the LNA before ICP (STD LNA) and after ICP etching (ICP LNA) are shown in Fig. 6(a). S_{11} is below -17 dB for the STD LNA and -11 dB for the ICP LNA over the band of interest (5.15–5.825 GHz). In addition, the calculated S_{11} by (7) is close to the measured S_{11} , which verifies the validity of our proposed theory. The good input match ($< -10 \text{ dB}$) between 5.15–5.825 GHz indicates that both LNAs are suitable for multistandard applications [3]. The “blue-shift” of the frequency band may be due to the reduction of parasitic capacitance after ICP. The output buffer achieves excellent output matching over the band of measurement (1–10 GHz) in both cases.

Fig. 6(b) shows the measured gain (S_{21}) and reverse isolation (S_{12}) for both LNAs. The maximum S_{21} is 21 and 23 dB for the STD and ICP LNAs, respectively. That is, there is a 2-dB gain enhancement after ICP etching. Note that the voltage gain of the core amplifier is 6 dB higher than S_{21} because the output source follower drives a matched load [19]. The calculated S_{21} by (11) is close to the measured S_{21} , which verifies again the validity of our proposed theory. The isolation is better than 36.5 dB over the band of interest for the STD and ICP LNAs.

The NF performance measured by an ATN NP-5 system before and after ICP etching is shown in Fig. 6(c). Clearly, the reduction of NF can be achieved by backside ICP dry etching over the measured frequency range. The ICP LNA shows a relatively broad-band low-NF characteristic (below 2 dB) over the band of interest with a minimum NF as low as 1.78 dB at 5.4 GHz, which is again suitable for multistandard applications.

TABLE I
SUMMARY OF THE PRESENTED AND THE PREVIOUSLY REPORTED
STATE-OF-THE-ART 5-GHz-BAND CMOS CASCODE LNAs

Ref	Input Matching	NF (dB)	S_{21} (dB)	P_{dc} (mW)
This Work 0.25 μm CMOS	STD LNA 5.15–5.825 GHz ($S_{11} < -17 \text{ dB}$) On chip	2.26@5.2GHz 2.28@5.4GHz 2.41@5.7GHz	21	30
	ICP LNA 5.15–5.825 GHz ($S_{11} < -11 \text{ dB}$) On chip	1.83@5.2GHz 1.78@5.4GHz 1.88@5.7GHz	23	
[1] 0.18 μm CMOS	5.725–5.825 GHz Off chip	7 @ 5.2GHz 1.8 @ 5.75GHz	14.1	21.6
[2] 0.25 μm CMOS	5.15–5.35 GHz On chip	2.5 @ 5.15GHz	16	48
[3] 0.18 μm CMOS	5.15–5.35 GHz ($S_{11} < -12 \text{ dB}$) Off chip 5.25–5.825 GHz ($S_{11} < -8 \text{ dB}$)	@ 5.15–5.35GHz 4.5 @ 5.725–5.825GHz	18	n/a
[4] 0.24 μm CMOS	5.15–5.35 GHz Off chip	4.8 @ 5.15GHz	18*	7.2

* : voltage gain

This is in contrast with [1] where NF degrades rapidly as frequency deviated from 5.75 GHz [see Fig. 6(c)], although the state-of-the-art NF of 1.8 dB at 5.75 GHz in 0.18- μm CMOS technology is achieved. Table I is a summary of the presented and the previously reported state-of-the-art 5-GHz-band CMOS cascode LNAs. The NF of our ICP LNA for multistandard WLAN applications is 1.83 dB at 5.2 GHz and 1.88 dB at 5.7 GHz, respectively. The former is the state-of-the-art result and the latter is comparable to previous report on a 0.18- μm cascode CMOS LNA with *off-chip bonding wire inductors* [1]. Namely, the simple ICP etching can enhance the performance of 0.25- μm CMOS LNA with on-chip inductors to parallel and even exceed the performance of 0.18- μm CMOS LNA with off-chip inductors.

B. Micromachined 4-GHz CMOS VCO

Fig. 3(a) shows the schematic diagram of the 4-GHz CMOS LC VCO. The VCO can operate from 3.9 to 4.2 GHz, as shown in Fig. 7(a). Fig. 7(b) shows that the phase noise can be suppressed by 3 dB after backside ICP dry etching. Table II is a summary of the state-of-the-art 4–6-GHz CMOS LC VCO, in which the “FOM” means the widely accepted figure-of-merit defined as follows [20]:

$$\text{FOM} = 10 \log \left[\left(\frac{\Delta f}{f_o} \right)^2 \cdot P_{DC} \right] + L(\Delta f) \quad (\text{dBc/Hz}) \quad (18)$$

where f_o means carrier frequency, Δf means offset frequency, and $L(\Delta f)$ means phase noise. According to Table II, the FOM of our VCO after ICP dry etching is the best among the 4–6-GHz CMOS LC VCO with a practical tuning range ($> \sim 5\%$).

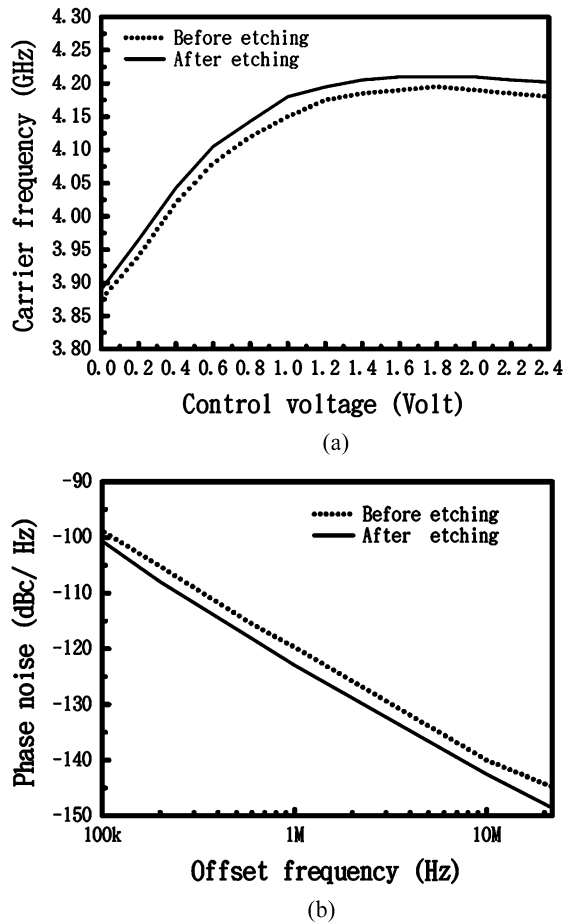


Fig. 7. Measured: (a) tuning range and (b) phase noise of the 4-GHz CMOS LC VCO.

TABLE II
SUMMARY OF THE PRESENTED AND THE PREVIOUSLY REPORTED
STATE-OF-THE-ART 4–6-GHz CMOS LC VCO

	P_{DC} (mW)	Carrier frequency (GHz)	Phase noise at 1MHz (dBc/Hz)	FOM (dBc/Hz)
This work 0.25 μm CMOS	7	4.2 GHz	-122.94	-186.9
[21] 0.25 μm CMOS	7.5	4 GHz	-117	-180.3
[22] 0.18 μm CMOS	5.9	5.6 GHz	-116.7	-184

VI. CONCLUSION

First, a CMOS process compatible backside ICP dry etching technology to form deep trenches underneath the inductors of RF ICs is developed to enhance the performance of RF ICs with on-chip inductors. Second, the experimental results show the 5.15–5.825-GHz 0.25- μm CMOS LNA with on-chip inductors after ICP etching not only has a minimum NF (1.78 dB) comparable to that (1.8 dB) of the previous state-of-the-art 0.18- μm cascode CMOS LNA [1] with off-chip bond wire inductors, but

also has a wider low NF frequency range than [1]. The FOM of the VCO after ICP etching is the best among the 4–6-GHz CMOS LC VCO with a practical tuning range ($>\sim 5\%$). Finally, the CMOS process compatible ICP technology is also believed to increase the isolation between RF/analog and digital circuits and thus paves a way for SOC.

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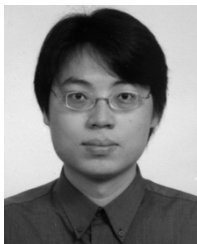
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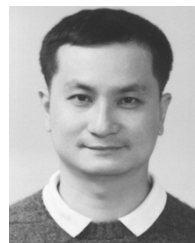
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