

A Dual-Mode Truly Modular Programmable Fractional Divider Based on a 1/1.5 Divider Cell

Yu-Che Yang, Shih-An Yu, Tao Wang, and Shey-Shi Lu

Abstract—A divide-by-1/1.5 divider cell using a dual edge-trigger technique is proposed. Based on this divider cell, a dual-mode programmable divide-by- X circuit is demonstrated in 0.18- μm CMOS technology, where $X = P$ or $P.5$ in one mode and $2P$ or $2P+1$ in the other mode with $P = 128\text{--}255$. When operated in the divide-by- $2P/2P+1$ mode, this circuit outputs a signal with 50% duty cycle. Theoretically, P can be any arbitrary and programmable integer.

Index Terms—50% duty cycle and phase-locked loop (PLL), fractional divider, programmable divider.

I. INTRODUCTION

CONVENTIONAL fractional- N phase-locked loops (PLLs) are mainly based on a fractional divider composed of an integer- N divider and a Δ - Σ modulator [1], [2], where the former is modulated by the latter so that the desired fractional division ratio is obtained. However, since the intrinsic division ratio of the divider is still an integer, the quantization noise is inevitably introduced, and hence, contributes to the total phase noise of the PLL. To suppress the quantization noise, a fractional divider with intrinsically fractional division ratios, which we call intrinsic fractional divider for the ease of later discussions, is needed.

In this work, a novel 1/1.5 divider cell is proposed. Based on this divider cell, an intrinsic fractional divider with a dividing range of 128–255.5 and a step size of 0.5 was realized in 0.18- μm CMOS technology. It is predicted that the quantization noise in a fractional- N PLL using this intrinsic fractional divider in conjunction with a Δ - Σ modulator is 6 dB smaller than that in a conventional fraction- N PLL due to the intrinsic fractional modulus.

There is also a need of integer- N dividers with 50% duty-cycle [3]. In fact, a divide-by-three circuit with 50% duty cycle has been published [3]. However, to our knowledge, a 50% duty cycle divide-by-odd number circuit with the odd number other than three has not been reported. Another important application of the proposed 1/1.5 divider cell is in generating 50% duty-cycle output signals from a divide-by- N circuit, where N is an arbitrary integer. In this letter, a 50% duty cycle programmable divide-by- N circuit ($N = 256\text{--}511$) as well as a

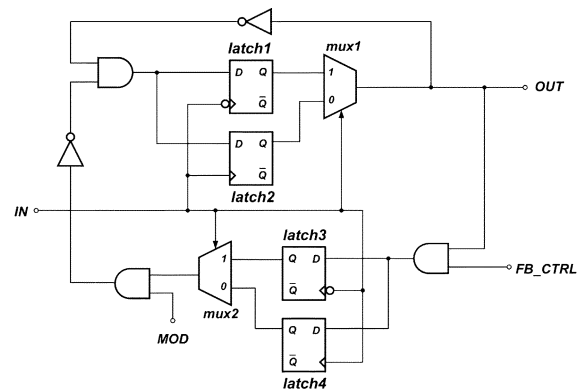


Fig. 1. Schematic of 1/1.5 divider cell.

50% duty cycle divide-by-three circuit based on the 1/1.5 divider cell is demonstrated. Theoretically, N can be any arbitrary and programmable integer.

II. CIRCUIT DESIGN

A. 1/1.5 Divider Cell

The key operating principle of the 1/1.5 divider cell is to trigger the divider either on the rising or falling edge of the input signal. Fig. 1 shows the schematic of the 1/1.5 divider cell, which consists of two multiplexers (mux), four latches, and three AND gates. This structure is similar to the 2/3 divider cell in [4], but the serially-connected latches in [4] are replaced by parallel-connected latches in combination with a multiplexer. One of the latches is enabled by the positive edge, and the other is enabled by the negative edge of the input signal with their outputs selected by the multiplexer. When MOD and FB_CTRL are both high, the divider is in the divide-by-1.5 mode with its timing chart illustrated in Fig. 2, where the operation of divide-by-1.5 can be clearly traced. When either MOD or FB_CTRL is low, the output signal of latch1 remains high (or low) while the latch2 stays low (or high) and the feedback signal from the bottom of Fig. 1 is always high. Thus, the OUT simply tracks the input signal, i.e., divided by 1. The source-coupled-logic (SCL) configuration [4] is adopted for the latch used in the 1/1.5 divider because of its high-frequency characteristic resulted from the constant supply current and differential voltage swing operation.

B. Dual-Mode Programmable Fractional Divider

Based on the 1/1.5 divider cell, a dual-mode truly modular programmable fractional divider can be implemented. The first

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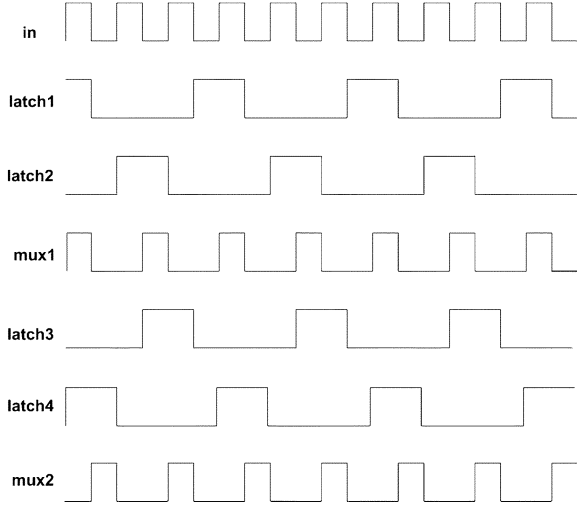


Fig. 2. Timing chart of the 1/1.5 divider cell in divide-by-1.5 mode.

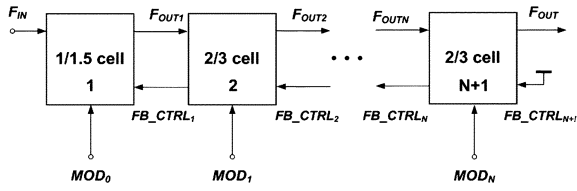


Fig. 3. Core of the proposed divider (divider core).

mode of this divider is to achieve intrinsic fractional modulus and the other is to generate 50% duty-cycle output signals in all integer modulus. The core of the programmable divider (Divider Core) is depicted in Fig. 3. The operation of this architecture is similar to the one described in [4] except that an additional 1/1.5 divider cell is placed in front of a chain consisting of 2/3 divider cells. The period of the output signal T_{OUT} can be shown to be

$$T_{OUT} = (2^N + 2^{N-1} \cdot MOD_N + \dots + 2 \cdot MOD_2 + MOD_1 + 0.5 \cdot MOD_0) \cdot T_{IN} \quad (1)$$

where T_{IN} is the period of the input signal and $MOD_0, \dots,$ and MOD_N are the modulus control signals for the divider cells. From (1), it can be seen that the division ratio ranges from 2^N to $2^{N+1} - 0.5$ with a step size of 0.5 (a fractional number). For a Δ - Σ modulator fractional divider, the output frequency is

$$f_{out} = \frac{f_{in}}{N_0 + b(t)} \quad (2)$$

where f_{out} is the divider output frequency, f_{in} is the input frequency, N_0 is a fixed ration, and $b(t)$ is the bit stream generated from the Δ - Σ modulator, which is a modulated form of a fractional number k . The average output frequency is

$$\overline{f_{out}} = \frac{f_{in}}{N_0 + k}. \quad (3)$$

Assuming $M = N_0 + k$, the frequency error caused by dithering

$$\Delta f = f_{out} - \overline{f_{out}} \quad (4)$$

$$\Delta f = \frac{f_{in}}{M} \cdot \left[\frac{1}{1 + \frac{q(t)}{M}} - 1 \right] \quad (5)$$

$$\Delta f \approx \overline{f_{out}} \cdot \frac{-q(t)}{M} \quad (6)$$

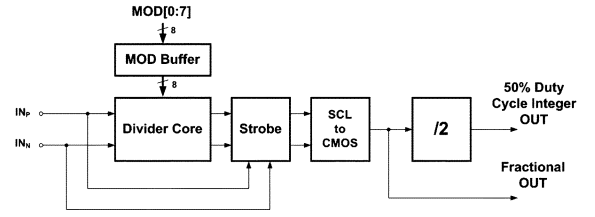


Fig. 4. Complete schematic of the programmable divider.

where $q(t) = b(t) - k$. Consider how the frequency dithering is transformed to phase noise

$$\Delta f = \frac{\Delta\omega}{2\pi} = \frac{1}{2\pi} \frac{d\phi(t)}{dt} \quad (7)$$

$$S_{\Delta f} = \left(\frac{1}{2\pi} \right)^2 \cdot S_{\frac{d\phi}{dt}} \quad (8)$$

$$S_{\Delta f} = F\{\Delta f \Delta f^*\} \quad (9)$$

$$S_{\Delta f} = F\left\{ \left(\frac{d\phi}{dt} \right) \left(\frac{d\phi}{dt} \right)^* \right\} \quad (10)$$

where $S_{\Delta f}$ represents the power spectral density (PSD) of Δf and $F\{\}$ denotes Fourier transform. According to the differentiate rule of Fourier transform

$$S_{\Delta f} = \left(\frac{1}{2\pi} \right)^2 (2\pi f)^2 \cdot S_{\phi} = f^2 S_{\phi}. \quad (11)$$

Based on (6), $S_{\Delta f}$ can be written as

$$S_{\Delta f} = \overline{f_{out}}^2 \cdot \left(\frac{1}{M} \right)^2 \cdot S_{q(t)}. \quad (12)$$

Combine the previous two equations

$$S_{\phi} = \overline{f_{out}}^2 \cdot \frac{1}{M^2} \cdot \frac{1}{f^2} \cdot S_{q(t)}. \quad (13)$$

We can relate the $q(t)$ with the DSM output bit stream $b(t)$

$$S_{\phi} = \frac{1}{M^2} \cdot \left(\frac{\overline{f_{out}}^2}{f} \right) \cdot (F\{|b(t) - k|^2\}). \quad (14)$$

Clearly, the phase noise contributed by the fractional divider can be lowered by 6 dB if $b(t)$ with a step size of 1 is replaced by $b(t)$ with a step size of 0.5. The complete schematic of the dual mode programmable divider is shown in Fig. 4. A strobe circuit, consisting of two parallel latches and a mux, is connected at the output of the divider core in order to resynchronize the output signal of the divider core by the input signal, and thus lowering the jitter accumulated in the divider core. A SCL-to-CMOS circuit translates the source coupled logic to standard CMOS logic signals (fractional OUT) and functions as an output buffer. The other mode of the proposed programmable divider is to divide the input signal by an integer with a 50% duty-cycle even when the division ratio is an odd integer. This is achieved by dividing the Fractional OUT signals by two as shown in Fig. 4. With this additional divide-by-two circuit, the output period are now two times of T_{OUT} , and hence the division ratio becomes $2^{N+1} - 2^{N+2} - 1$ but with 50% duty cycle output signals even with an odd division ratio.

III. MEASURED RESULTS

To verify the function of the 1/1.5 divider cell, the dual mode programmable fractional divider as well as the 50% duty cycle divide-by-three circuit is implemented in a standard 0.18- μm

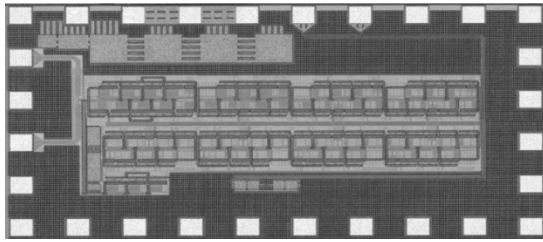


Fig. 5. Die photo of dual mode programmable fractional divider.

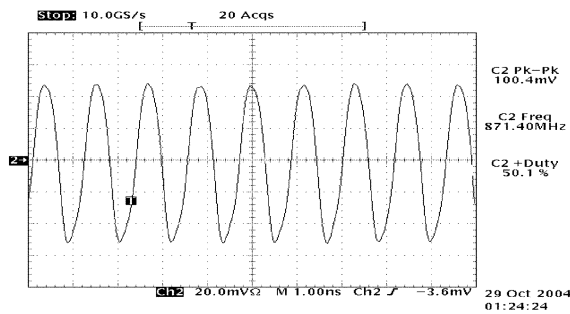


Fig. 6. Measured 50% duty cycle output waveform (871 MHz) of divide-by-three circuit when a 2.6-GHz input signal is applied. Note that 50% duty cycle is achieved.

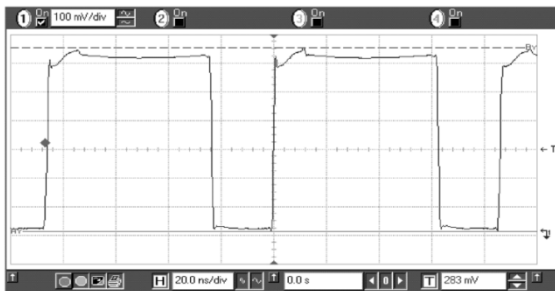


Fig. 7. Measured output waveform (10.02 MHz) of the programmable divider with modulus= 255.5 when a 2.56-GHz input signal is applied.

CMOS process. Fig. 5 shows the die photo of the dual mode programmable fractional divider. The divide-by-three circuit is operated at 1.8 V while the dual mode programmable fractional divider at 2.2 V.

When an input signal with a 2.6-GHz frequency is applied to the divide-by-three circuit, the measured output waveform is shown in Fig. 6, where a signal with one-third frequency (871 MHz) of the input signal (2.6 GHz) is observed. It is also clear that the 50% duty cycle is obtained at the same time. The programmable divider was implemented with 8 b, including one 1/1.5 divider cell and seven 2/3 divider cells. According to (1), the division range is from 128 to 255.5 in the fractional division mode and from 256 to 511 in the integer division mode. Fig. 7 shows output waveform of the programmable divider when the modulus of the divider is set to be 255.5 and an input signal with a 2.56-GHz frequency is applied. From Fig. 7, it can be seen the output frequency is 10.02 MHz, corresponding to the right division ratio. Fig. 8 shows output waveform of the programmable divider when the modulus of the divider is set to be 511 and an input signal with a 1.28-GHz frequency is applied. The output frequency is 2.504 MHz, corresponding to 1/511 of the input

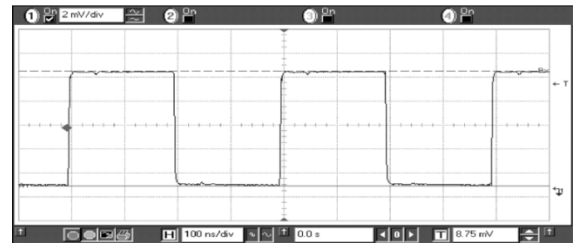


Fig. 8. Measured output waveform (2.504 MHz) of the programmable divider with modulus= 511 when a 1.28-GHz input signal is applied.

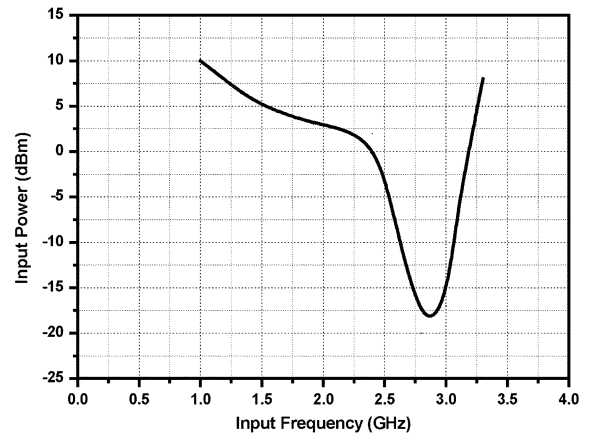


Fig. 9. Measured input sensitivity of the programmable divider.

frequency. Note that 50% duty cycle is achieved. The input sensitivity curve of the programmable divider is shown in Fig. 9. The measured operating range is from 1 to 3.3 GHz.

IV. CONCLUSION

A proto-type dual mode programmable fractional divider based on 1/1.5 divider cell is demonstrated in 0.18- μm CMOS technology. In the fractional division mode, input signals up to 3.3 GHz can be divided by 128–255.5 with a step size of 0.5. Phase noise contributed by this intrinsic fractional divider in conjunction with a Δ - Σ modulator in a PLL is expected to be lowered by 6 dB compared to the conventional integer divider in conjunction with a Δ - Σ modulator. In the integer division mode, 50% duty cycle output signals can be obtained after dividing the input signal by 256–511 with a step size of 1. A divide-by-three circuit with 50% duty cycle output signals based on 1/1.5 divider cell is also reported.

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